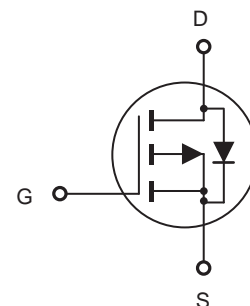


P-Channel Enhancement Mode Field Effect Transistor

FEATURES

- -60V, -2.4A, $R_{DS(ON)} = 135m\Omega$ @ $V_{GS} = -10V$.
 $R_{DS(ON)} = 180m\Omega$ @ $V_{GS} = -4.5V$.
- High dense cell design for extremely low $R_{DS(ON)}$.
- Rugged and reliable.
- Lead free product is acquired.
- SOT-89 package.



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-2.4	A
Drain Current-Pulsed ^a	I_{DM}	-10	A
Maximum Power Dissipation	P_D	1.25	W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	100	$^\circ\text{C/W}$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

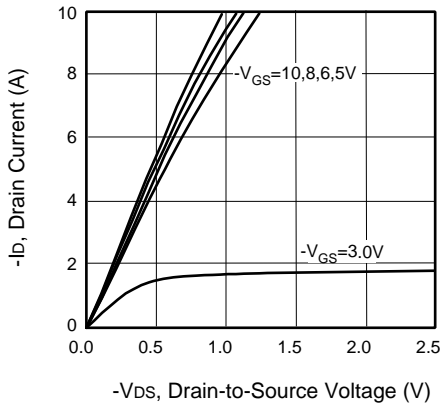
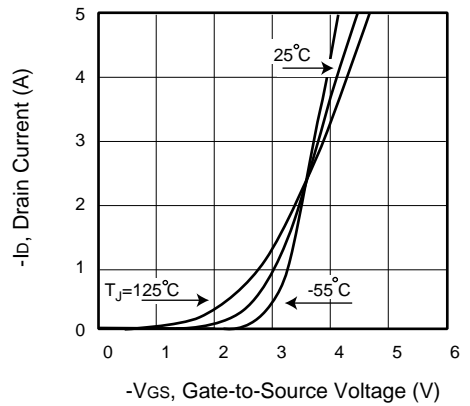
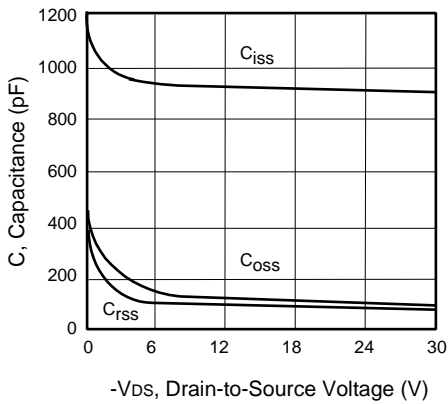
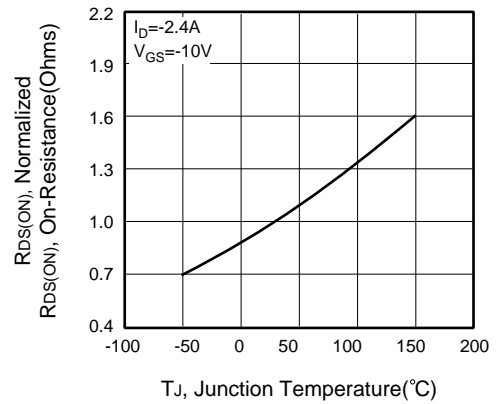
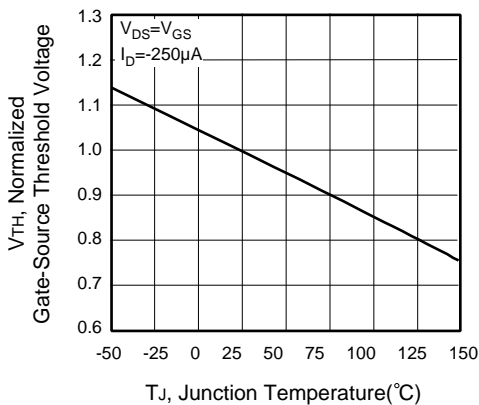
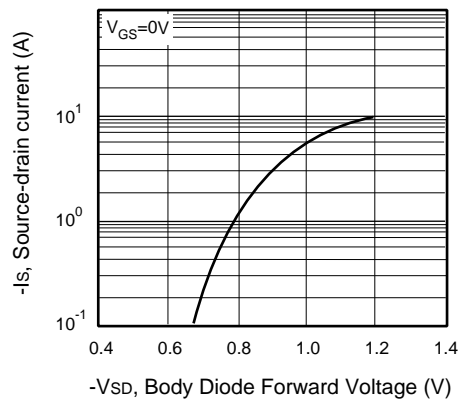
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V, V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -2.4A$		105	135	$m\Omega$
		$V_{GS} = -4.5V, I_D = -1.9A$		135	180	$m\Omega$
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = -30V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		890		μF
Output Capacitance	C_{oss}			90		μF
Reverse Transfer Capacitance	C_{rss}			85		μF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30V, I_D = -1A,$ $V_{GS} = -10V, R_{GEN} = 6\Omega$		13	26	ns
Turn-On Rise Time	t_r			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			39	78	ns
Turn-Off Fall Time	t_f			13	26	ns
Total Gate Charge	Q_g	$V_{DS} = -30V, I_D = -2.4A,$ $V_{GS} = -10V$		11.2	14.8	nC
Gate-Source Charge	Q_{gs}			2.6		nC
Gate-Drain Charge	Q_{gd}			1.8		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S				-2.4	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = -1.3A$			-1.2	V

Notes :

a.Repetitive Rating : Pulse width limited by maximum junction temperature.

b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

c.Guaranteed by design, not subject to production testing.


Figure 1. Output Characteristics

Figure 2. Transfer Characteristics

Figure 3. Capacitance

Figure 4. On-Resistance Variation with Temperature

Figure 5. Gate Threshold Variation with Temperature

Figure 6. Body Diode Forward Voltage Variation with Source Current

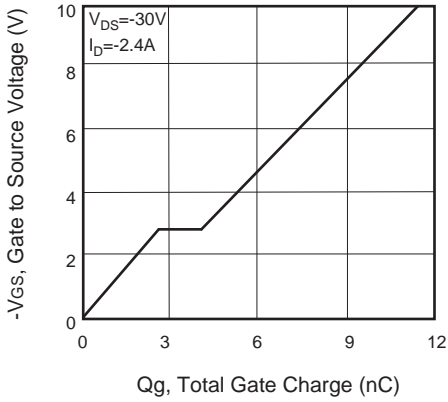


Figure 7. Gate Charge

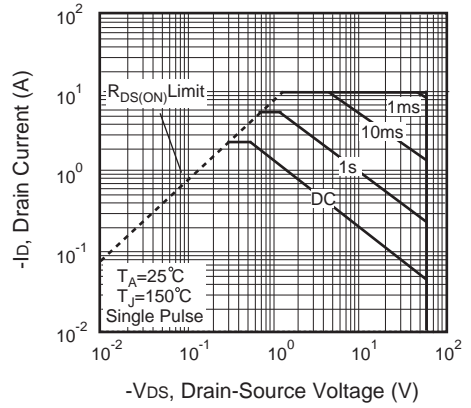


Figure 8. Maximum Safe Operating Area

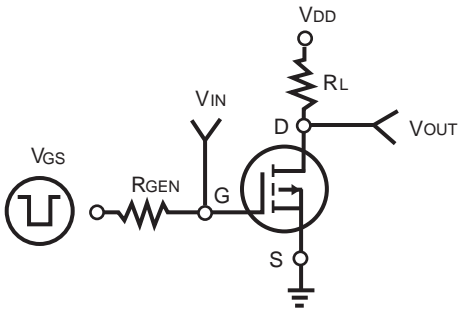


Figure 9. Switching Test Circuit

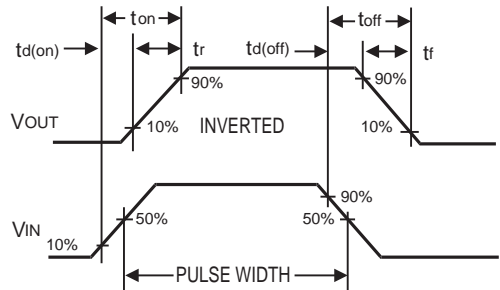


Figure 10. Switching Waveforms

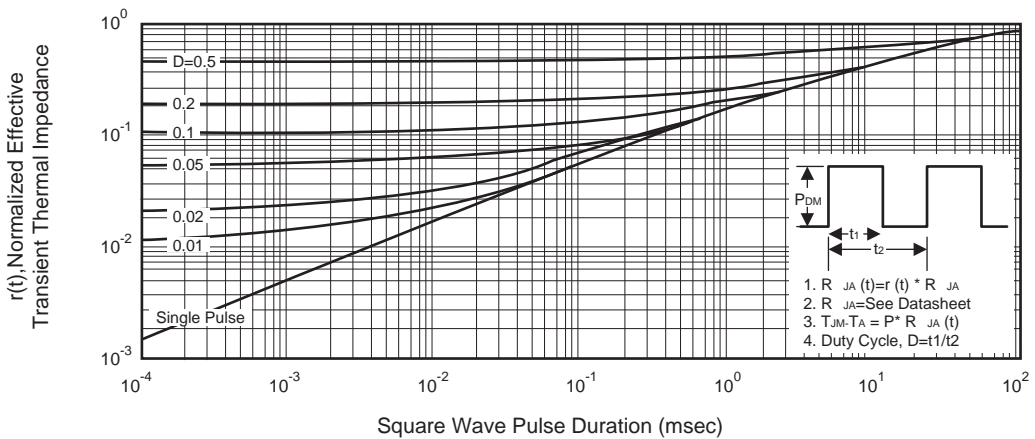
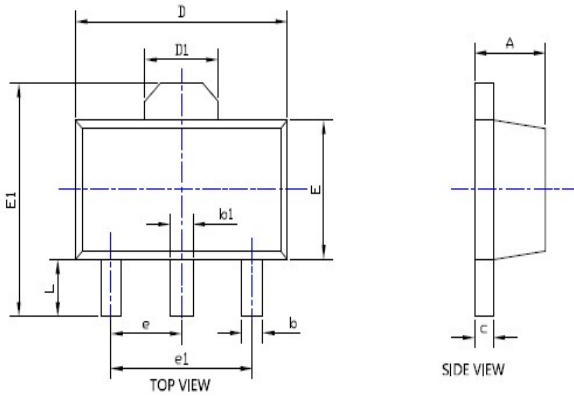
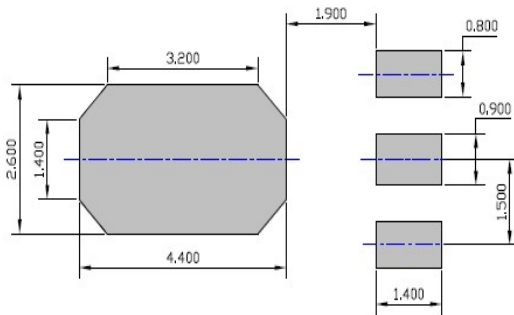


Figure 11. Normalized Thermal Transient Impedance Curve

■ SOT-89 Package information


SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.055	0.059	0.063	1.400	1.500	1.600
b	0.014	---	0.020	0.350	---	0.520
b1	0.016	---	0.023	0.400	---	0.580
c	0.014	---	0.017	0.350	---	0.440
D	0.173	0.177	0.181	4.400	4.500	4.600
D1	0.061REF			1.550REF		
E	0.093	0.096	0.100	2.350	2.450	2.550
E1	0.155	---	0.167	3.940	---	4.250
e	0.059TYP			1.500TYP		
e1	0.118TYP			3.000TYP		
L	0.035	0.039	0.043	0.900	1.000	1.100



SUGGESTED SOLDER PAD LAYOUT

UNIT: mm

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.